

# DATA SHEET

## **TDF8704**

**8-bit high-speed analog-to-digital  
converter**

Product specification  
Supersedes data of April 1993  
File under Integrated Circuits, IC02

June 1994

**Philips Semiconductors**



**PHILIPS**

## 8-bit high-speed analog-to-digital converter

TDF8704

## FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- Extended temperature range (–40 to +85 °C)
- High signal-to-noise ratio over a large analog input frequency range (7.4 effective bits at 4.43 MHz full-scale input and at  $f_{\text{clk}} = 50$  MHz)
- Binary 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Stable internal reference voltage regulator included
- Power dissipation only 380 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

## APPLICATIONS

- General purpose high-speed analog-to-digital conversion for extended temperature applications
- Automotive
- RF, satellite and GPS (Global Positioning System)
- Medical
- General industrial
- Digital video (VCR, TV and satellite).

## GENERAL DESCRIPTION

The TDF8704T is an 8-bit high-speed analog-to-digital converter (ADC) for general industrial applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{CCA}}$	analog supply voltage		4.75	5.0	5.25	V
$V_{\text{CCD}}$	digital supply voltage		4.75	5.0	5.25	V
$V_{\text{CCO}}$	output stages supply voltage		4.75	5.0	5.25	V
$I_{\text{CCA}}$	analog supply current		–	37	46	mA
$I_{\text{CCD}}$	digital supply current		–	23	35	mA
$I_{\text{CCO}}$	output stages supply current		–	16	21	mA
ILE	DC integral linearity error		–	±0.4	±1	LSB
DLE	DC differential linearity error		–	±0.2	±0.5	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
$f_{\text{clk(max)}}$	maximum clock frequency		50	–	–	MHz
$P_{\text{tot}}$	total power dissipation		–	380	535	mW

## Note

1. Full-scale sine wave ( $f_i = 4.43$  MHz;  $f_{\text{clk}} = 50$  MHz).

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDF8704T/2	24	SO24L	plastic	SOT137-1	20 MHz
TDF8704T/4	24	SO24L	plastic	SOT137-1	40 MHz
TDF8704T/5	24	SO24L	plastic	SOT137-1	50 MHz

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BLOCK DIAGRAM

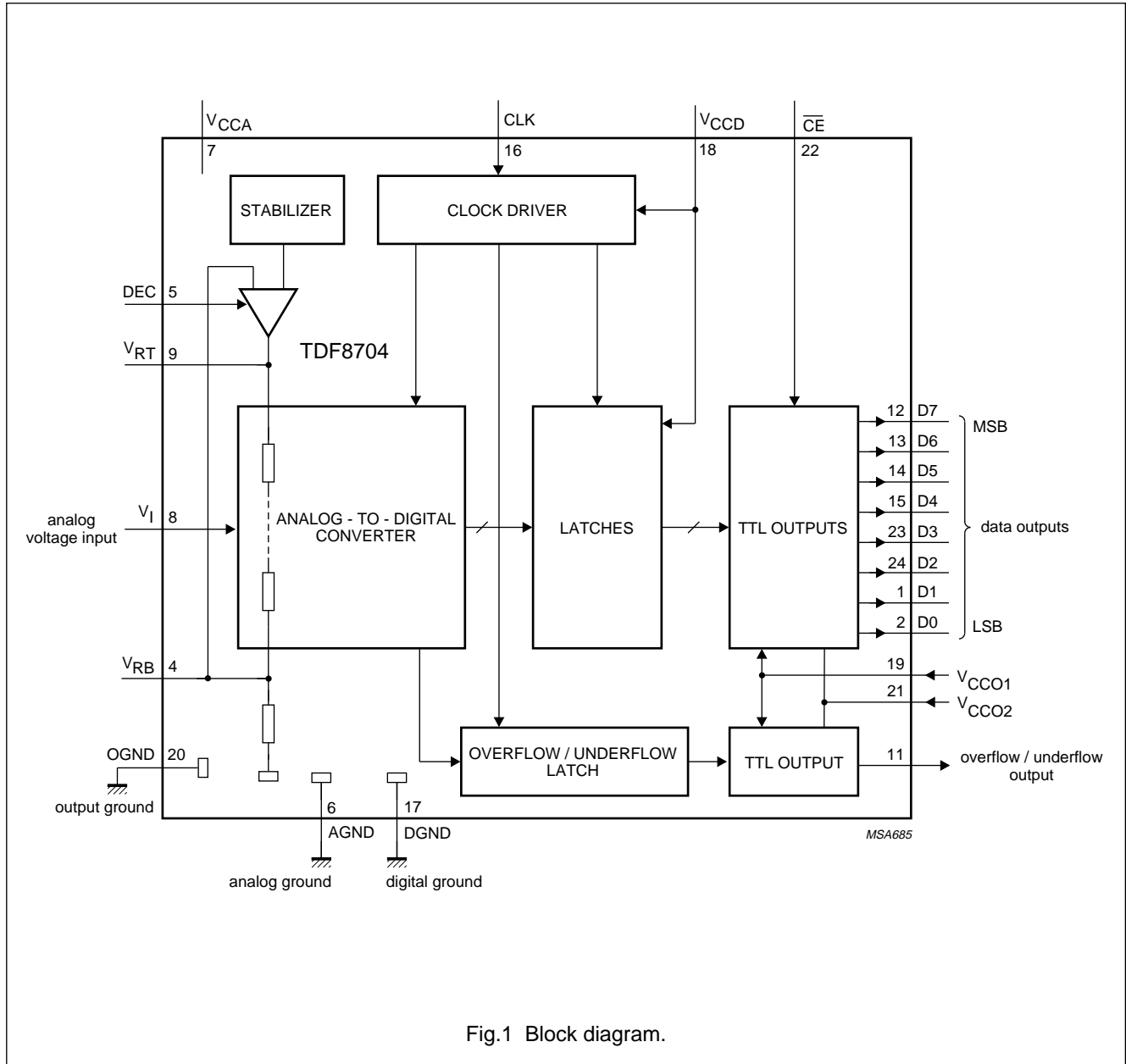


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V <sub>RB</sub>	4	reference voltage BOTTOM (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
AGND	6	analog ground
V <sub>CCA</sub>	7	analog supply voltage (+5 V)
V <sub>I</sub>	8	analog input voltage
V <sub>RT</sub>	9	reference voltage TOP (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V <sub>CCD</sub>	18	digital supply voltage (+5 V)
V <sub>CCO1</sub>	19	supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V <sub>CCO2</sub>	21	supply voltage for output stages 2 (+5 V)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

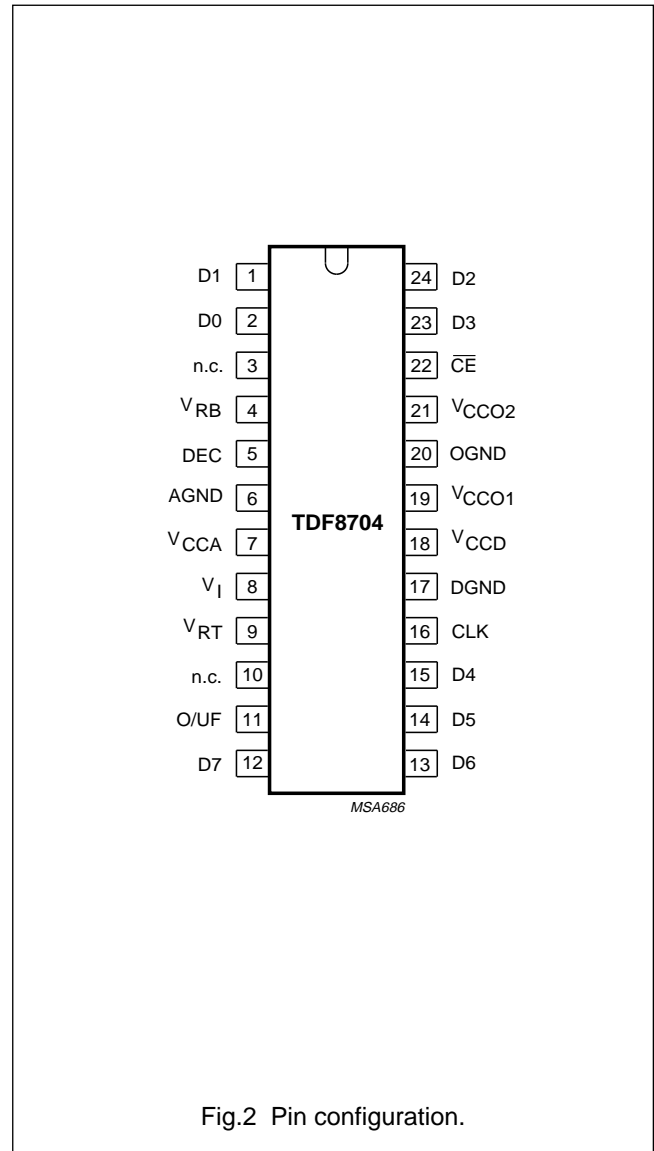


Fig.2 Pin configuration.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage		-0.3	+7.0	V
$V_{CCD}$	digital supply voltage		-0.3	+7.0	V
$V_{CCO}$	output stages supply voltage		-0.3	+7.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCA}$ and $V_{CCD}$		-1.0	+1.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCO}$ and $V_{CCD}$		-1.0	+1.0	V
$\Delta V_{CC}$	supply voltage differences between $V_{CCA}$ and $V_{CCO}$		-1.0	+1.0	V
$V_I$	input voltage	referenced to AGND	-0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	$V_{CCD}$	V
$I_o$	output current		-	10	mA
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		-40	+85	°C
$T_j$	junction temperature		-	+150	°C

**HANDLING**

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

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**CHARACTERISTICS (see Tables 1 and 2)**

$V_{CCA} = V_7$  to  $V_6 = 4.75$  to  $5.25$  V;  $V_{CCD} = V_{18}$  to  $V_{17} = 4.75$  to  $5.25$  V;  $V_{CCO} = V_{19}$  and  $V_{21}$  to  $V_{20} = 4.75$  to  $5.25$  V; AGND and DGND shorted together;  $V_{CCA}$  to  $V_{CCD} = -0.25$  to  $+0.25$  V;  $V_{CCO}$  to  $V_{CCD} = -0.25$  to  $+0.25$  V;

$V_{CCA}$  to  $V_{CCD} = -0.25$  to  $+0.25$  V;  $T_{amb} = -40$  to  $+85$  °C; typical readings taken at  $V_{CCA} = V_{CCD} = 5$  V and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{CCA}$	analog supply voltage		4.75	5.0	5.25	V
$V_{CCD}$	digital supply voltage		4.75	5.0	5.25	V
$V_{CCO}$	output stages supply voltage		4.75	5.0	5.25	V
$I_{CCA}$	analog supply current		–	37	46	mA
$I_{CCD}$	digital supply current		–	23	35	mA
$I_{CCO}$	output stages supply current	all outputs LOW	–	16	21	mA
<b>Inputs</b>						
CLOCK INPUT CLK (REFERENCED TO DGND)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{clk} = 0.4$ V	–400	–	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{clk} = 2.7$ V	–	–	100	$\mu$ A
		$V_{clk} = V_{CCD}$	–	–	300	$\mu$ A
$Z_I$	input impedance	$f_{clk} = 50$ MHz	–	2	–	k $\Omega$
$C_I$	input capacitance	$f_{clk} = 50$ MHz	–	4.5	–	pF
$V_I$ (ANALOG INPUT VOLTAGE REFERENCED TO AGND; SEE FIGS 3 AND 4 AND TABLE 1)						
$V_{I(B)}$	input voltage (BOTTOM)		1.21	1.25	1.29	V
$V_{I(0)}$	input voltage	output code = 0	1.42	1.48	1.51	V
$V_{os(B)}$	offset voltage (BOTTOM)	$V_{I(0)}$ to $V_{I(B)}$	210	225	240	V
$V_{I(T)}$	input voltage (TOP)		3.37	3.46	3.58	V
$V_{I(255)}$	input voltage	output code = 255	3.14	3.22	3.30	V
$V_{os(T)}$	offset voltage (TOP)	$V_{I(T)}$ to $V_{I(255)}$	225	240	255	V
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		1.69	1.74	1.79	V
$I_L$	load current on $V_{RT}$ and $V_{RB}$		–300	–	+300	$\mu$ A
$I_{IL}$	LOW level input current	$V_I = 1.25$ V	–	0	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_I = 3.46$ V	40	150	400	$\mu$ A
$Z_I$	input impedance	$f_i = 4.43$ MHz	–	10	–	k $\Omega$
$C_I$	input capacitance	$f_i = 4.43$ MHz	–	14	–	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT $\overline{CE}$ (REFERENCED TO DGND) SEE TABLE 2						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	$\mu$ A
<b>Reference resistance</b>						
$R_{ref}$	reference resistance	$V_{RT}$ to $V_{RB}$	–	200	–	$\Omega$
<b>Outputs</b>						
DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO DGND)						
$V_{OL}$	LOW level output voltage	$I_O = 1$ mA; $T_{amb} = 0$ to $+85$ °C	0	–	0.4	V
		$I_O = 1$ mA; $T_{amb} = 0$ to $-40$ °C	–	–	0.6	V
$V_{OH}$	HIGH level output voltage	$I_O = -0.4$ mA	2.7	–	$V_{CCD}$	V
$I_{OZ}$	output current in 3-state mode	$0.4$ V < $V_O$ < $V_{CCD}$	–20	–	+20	$\mu$ A
<b>Switching characteristics</b>						
CLOCK INPUT CLK (NOTE 1; SEE FIG.15)						
$f_{clk(max)}$	maximum clock frequency					
	TDF8704T/2		20	–	–	MHz
	TDF8704T/4		40	–	–	MHz
	TDF8704T/5		50	–	–	MHz
$t_{CPH}$	clock pulse width HIGH		7	–	–	ns
$t_{CPL}$	clock pulse width LOW		7	–	–	ns
<b>Analog signal processing</b>						
LINEARITY						
ILE	DC integral linearity error		–	$\pm 0.4$	$\pm 1.0$	LSB
DLE	DC differential linearity error		–	$\pm 0.2$	$\pm 0.5$	LSB
AILE	AC integral linearity error	note 2	–	–	$\pm 2.0$	LSB
BANDWIDTH ( $f_{clk} = 40$ MHz)						
B	–0.5 dB analog bandwidth (note 3)	full-scale sine wave	–	12	–	MHz
		75% full-scale sine wave	–	16	–	MHz
$t_{STLH}$	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.8; note 4	–	2.5	3.5	ns
$t_{STHL}$	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.8; note 4	–	3.0	4.0	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
HARMONICS ( $f_{\text{clk}} = 40 \text{ MHz}$ )							
$h_1$	fundamental harmonics (full scale)	$f_i = 4.43 \text{ MHz}$	–	–	0	dB	
$h_{\text{all}}$	harmonics (full scale); all components	$f_i = 4.43 \text{ MHz}$					
	second harmonics		–	–64	–60	dB	
	third harmonics		–	–58	–55	dB	
THD	total harmonic distortion	$f_i = 4.43 \text{ MHz}$	–	–56	–	dB	
SIGNAL-TO-NOISE RATIO							
S/N	signal-to-noise ratio	without harmonics; $f_{\text{clk}} = 40 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$	46	48	–	dB	
EFFECTIVE BITS; NOTE 5; SEE FIGS 9, 10 AND 11							
EB	effective bits TDF8704T/2	$f_{\text{clk}} = 20 \text{ MHz}$					
		$f_i = 1.25 \text{ MHz}$	–	7.8	–	bits	
		$f_i = 4.43 \text{ MHz}$	–	7.6	–	bits	
	effective bits TDF8704T/4	$f_{\text{clk}} = 40 \text{ MHz}$					
		$f_i = 4.43 \text{ MHz}$	–	7.5	–	bits	
		$f_i = 7.5 \text{ MHz}$	–	7.3	–	bits	
		$f_i = 10 \text{ MHz}$	–	7.0	–	bits	
	effective bits TDF8704T/5	$f_{\text{clk}} = 50 \text{ MHz}$					
		$f_i = 4.43 \text{ MHz}$	–	7.4	–	bits	
$f_i = 7.5 \text{ MHz}$		–	7.2	–	bits		
	$f_i = 10 \text{ MHz}$	–	6.9	–	bits		
TWO-TONE (NOTE 6)							
TTIR	two-tone intermodulation rejection	$f_{\text{clk}} = 40 \text{ MHz}$	–	–56	–	dB	
BIT ERROR RATE							
BER	bit error rate	$f_{\text{clk}} = 40 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$ ; $V_I = \pm 16 \text{ LSB at code 128}$	–	$10^{-11}$	–	times/ samples	
DIFFERENTIAL GAIN (NOTE 7)							
$G_{\text{diff}}$	differential gain	$f_{\text{clk}} = 20 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$	–	0.6	–	%	
DIFFERENTIAL PHASE (NOTE 7)							
$\Phi_{\text{diff}}$	differential phase	$f_{\text{clk}} = 40 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$	–	0.8	–	deg	



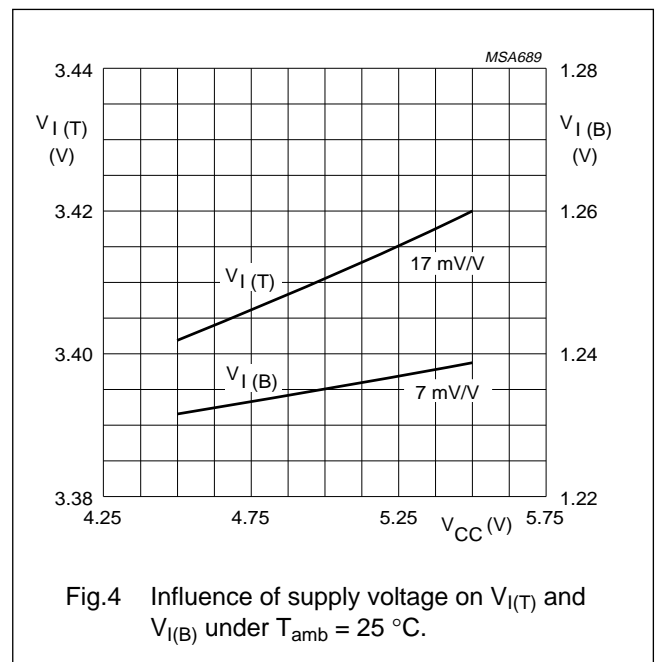
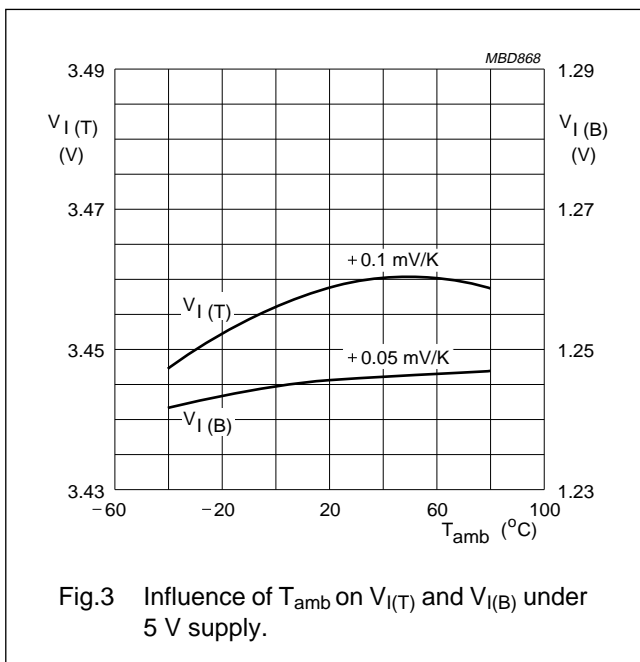
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Timing (note 8; see Figs 5 and 7; <math>f_{clk} = 50</math> MHz)</b>						
$t_{ds}$	sampling delay time		–	–	2	ns
$t_h$	output hold time		5	–	–	ns
$t_d$	output delay time		–	12	15	ns
<b>3-state output delay times (see Figs 6 and 7)</b>						
$t_{dZH}$	enable HIGH		–	6	10	ns
$t_{dZL}$	enable LOW		–	12	16	ns
$t_{dHZ}$	disable HIGH		–	50	54	ns
$t_{dLZ}$	disable LOW		–	10	14	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must be less than 1 ns.
2. Full-scale sine wave ( $f_i = 4.43$  MHz;  $f_{clk} = 50$  MHz).
3. Determined by beat frequency method on a reconstructed sine wave signal for no missing codes and no glitches.
4. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
5. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio:  $S/N = EB \times 6.02 + 1.76$  dB.
6. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
7. Measurement taken using video analyser VM700A.
8. Output data acquisition: the output data is available after the maximum delay time of  $t_d$ .



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**Table 1** Output coding and input voltage (typical values; referenced to AGND).

STEP	$V_{I(p-p)}$	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.48	1	1	0	0	0	0	0	0	0
0	1.48	0	0	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	3.46	0	1	1	1	1	1	1	1	1
Overflow	>3.46	1	1	1	1	1	1	1	1	1

**Table 2** Mode selection.

$\overline{CE}$	D7 TO D0	O/UF
1	high impedance	high impedance
0	active; binary	active

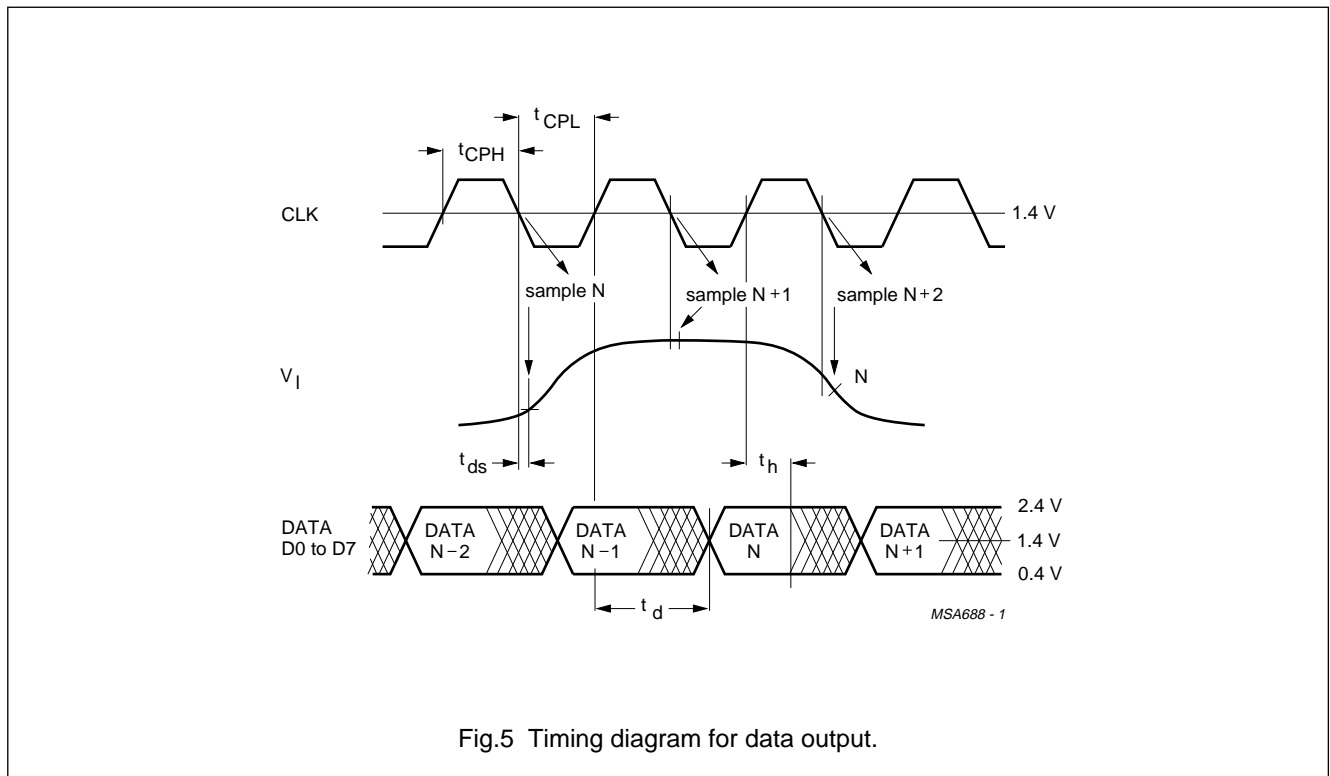
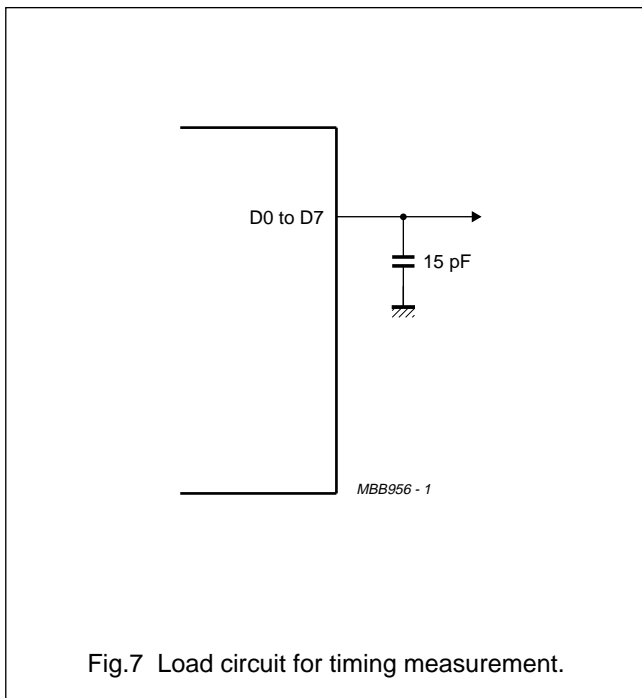
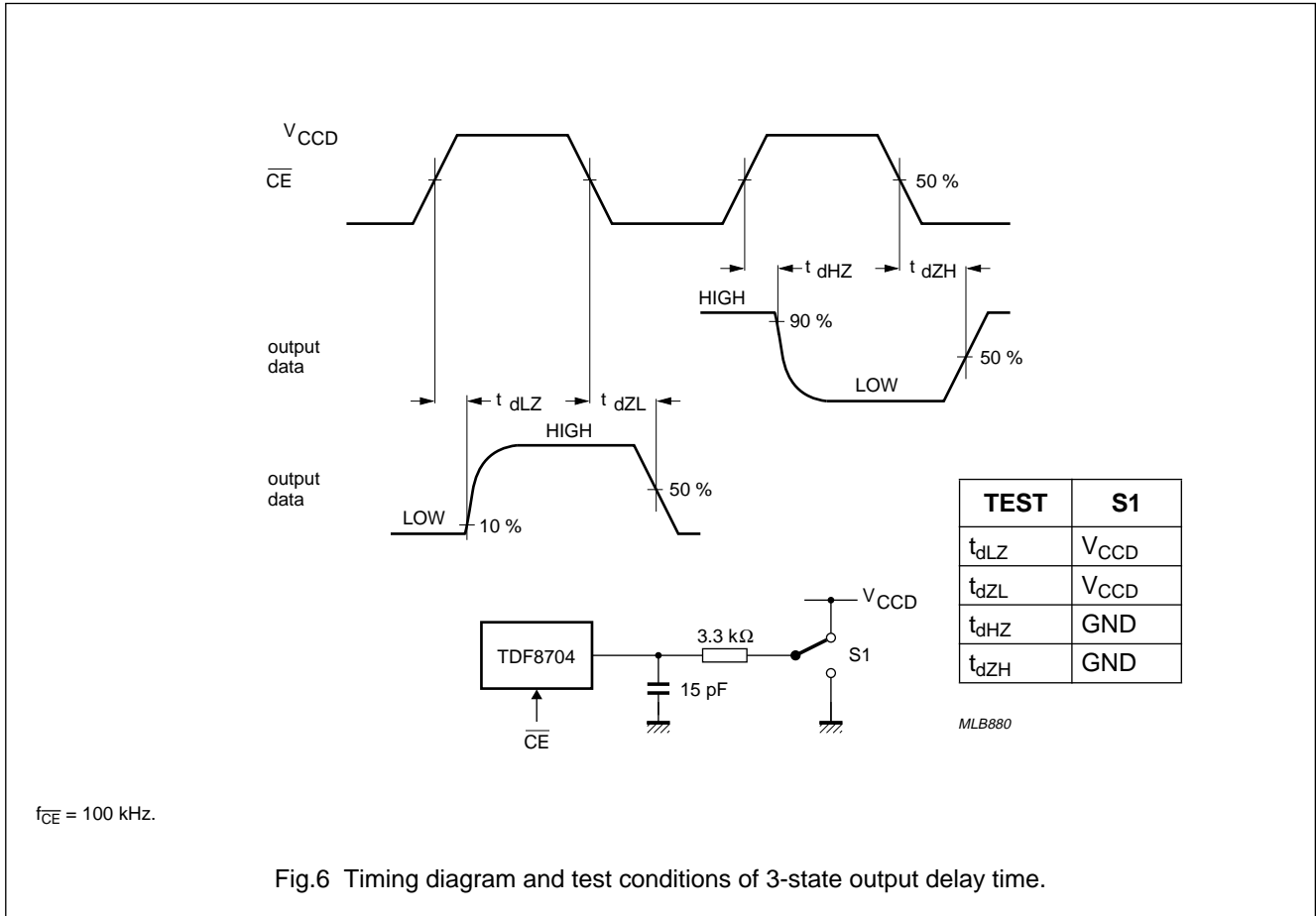


Fig.5 Timing diagram for data output.

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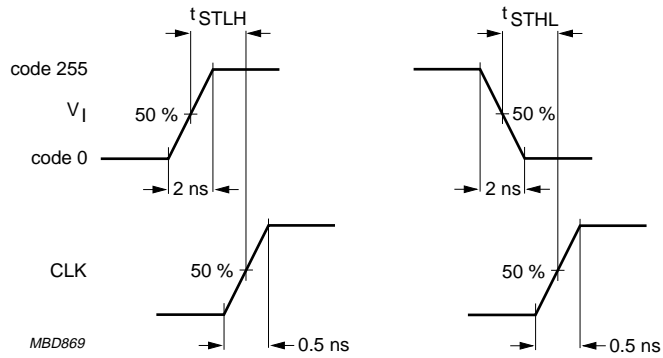
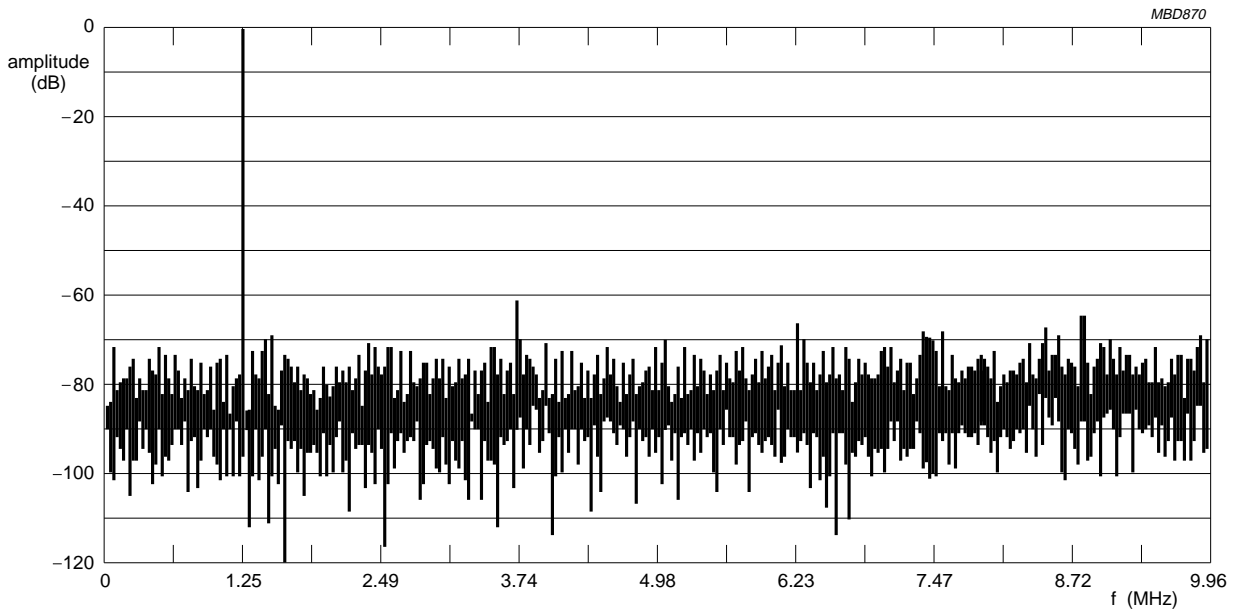


Fig.8 Analog input settling-time diagram.

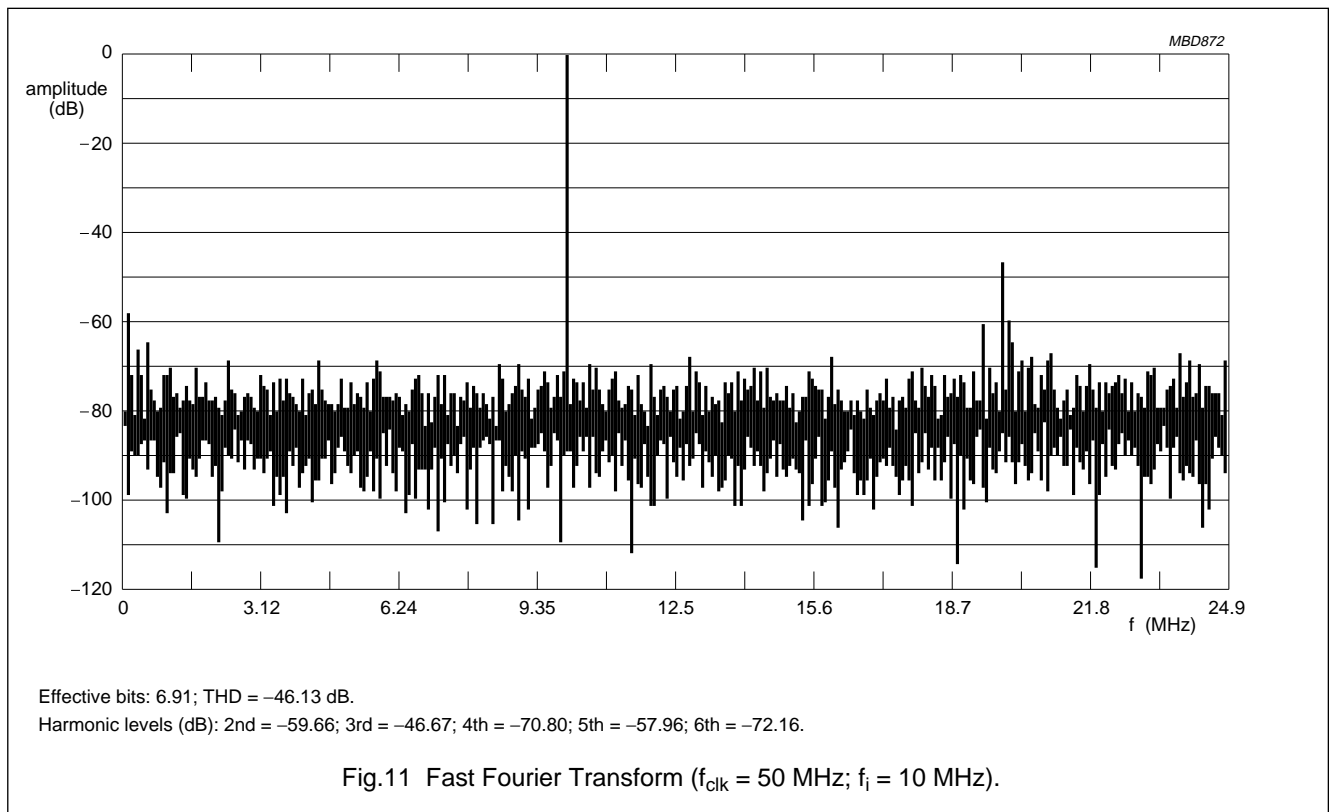
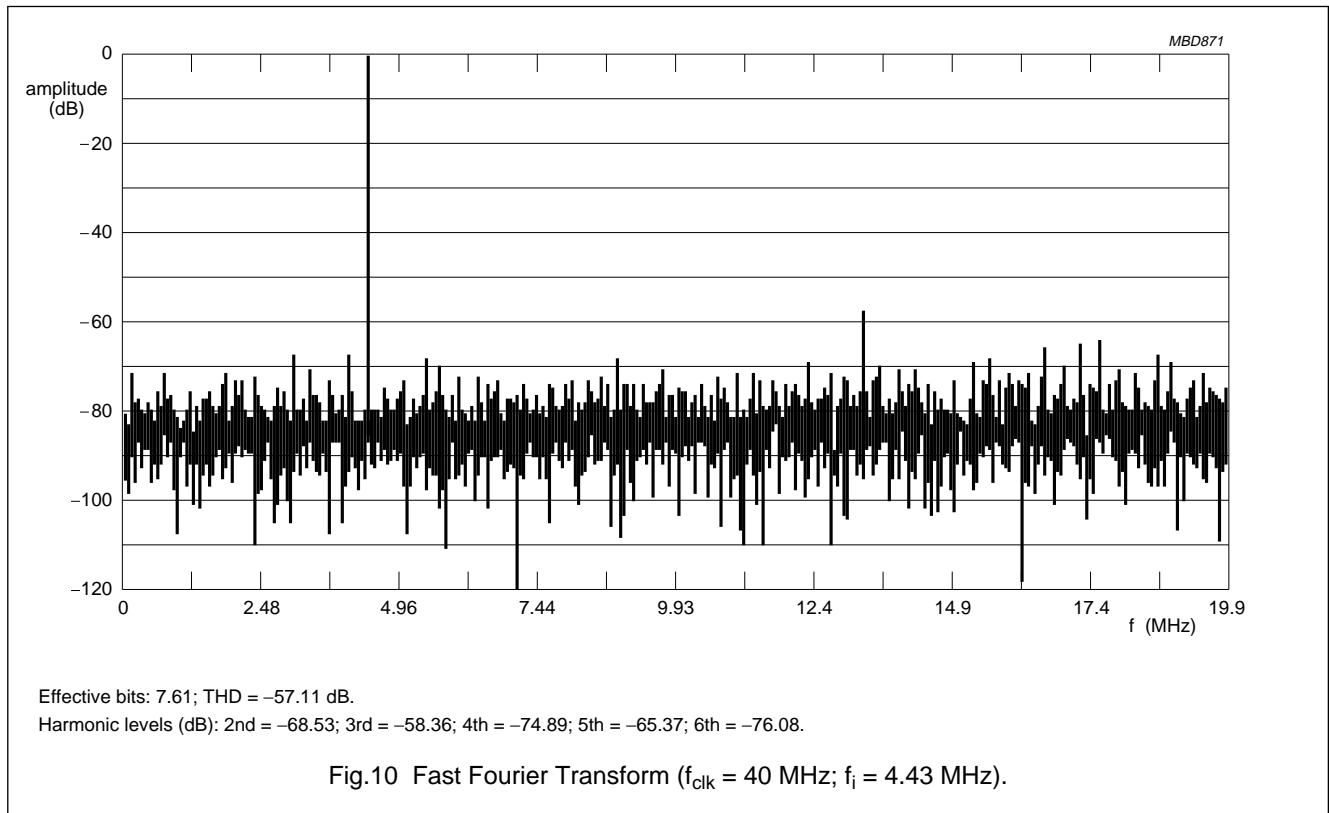


Effective bits: 7.89; THD = -61.05 dB.  
 Harmonic levels (dB): 2nd = -84.07; 3rd = -62.50; 4th = -92.01; 5th = -66.56; 6th = -101.15.

Fig.9 Fast Fourier Transform ( $f_{clk} = 20$  MHz;  $f_i = 1.25$  MHz).

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INTERNAL PIN CONFIGURATIONS

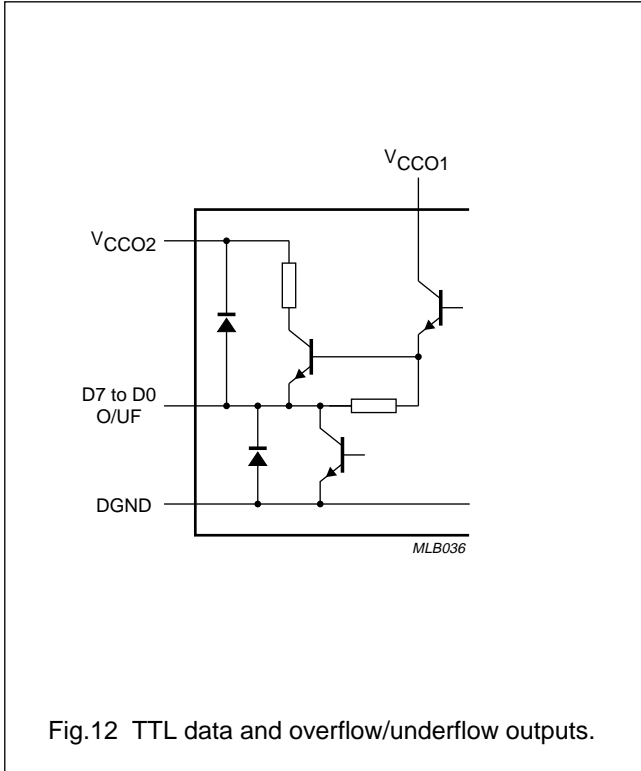


Fig.12 TTL data and overflow/underflow outputs.

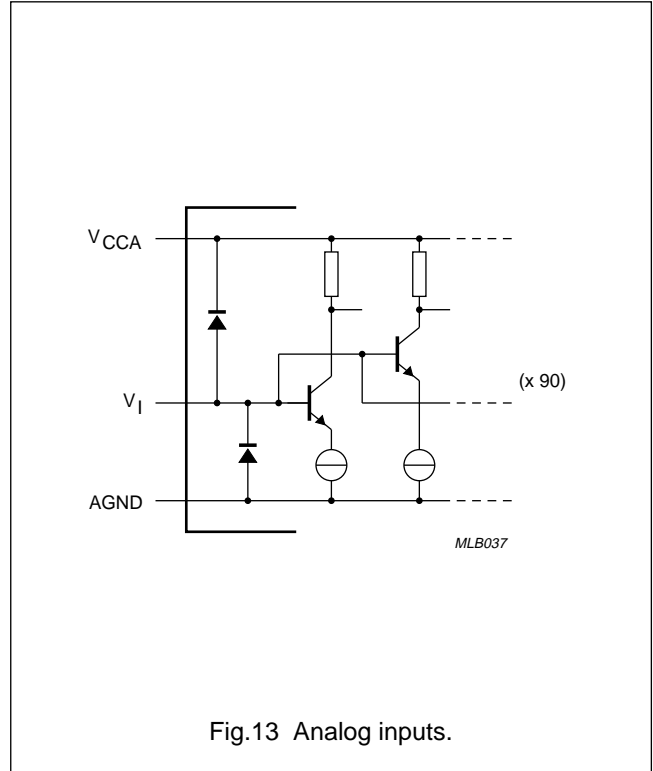


Fig.13 Analog inputs.

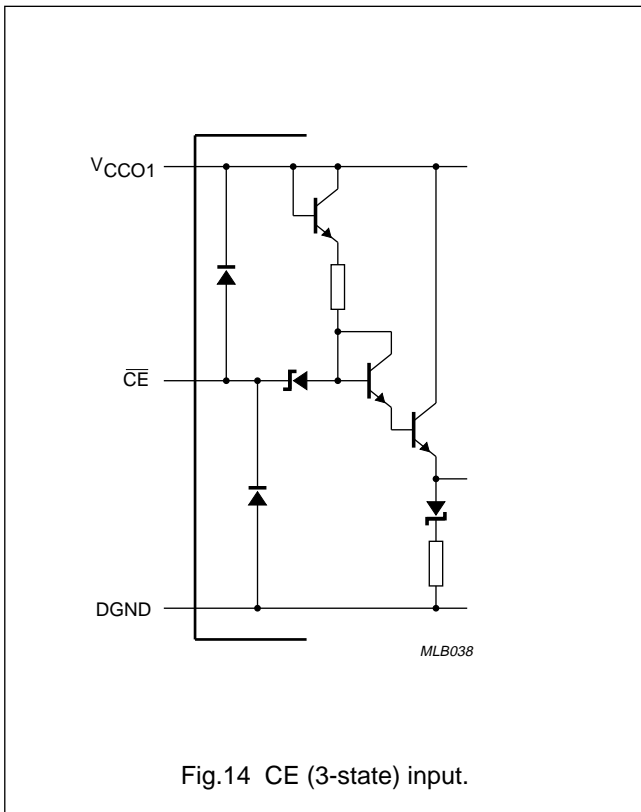


Fig.14 CE (3-state) input.

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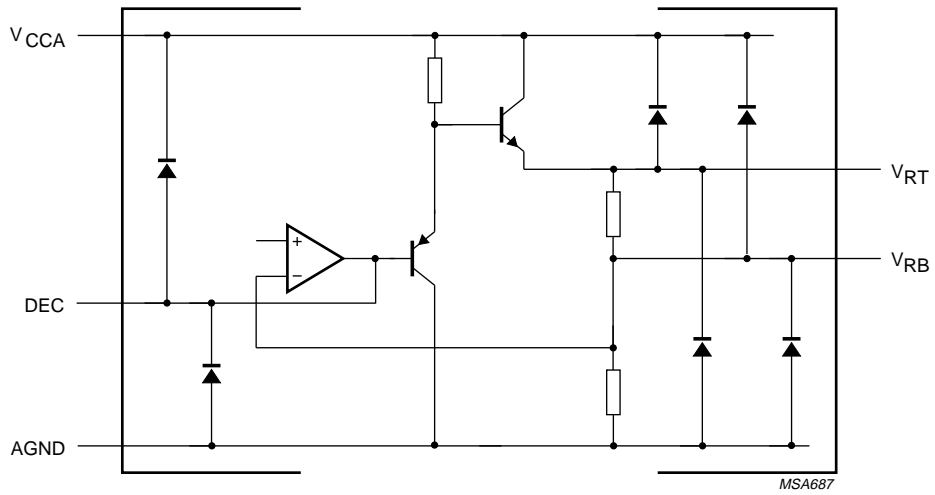


Fig.15  $V_{RB}$ ,  $V_{RT}$  and DEC.

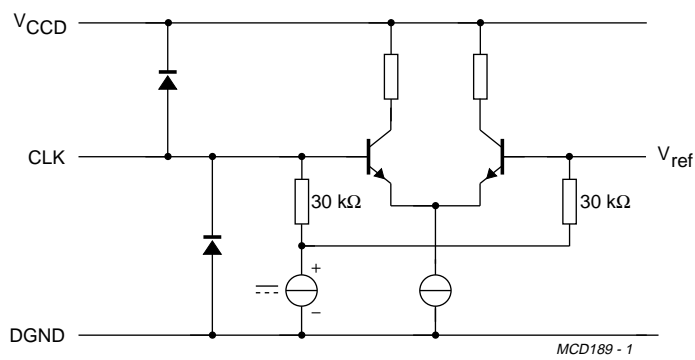
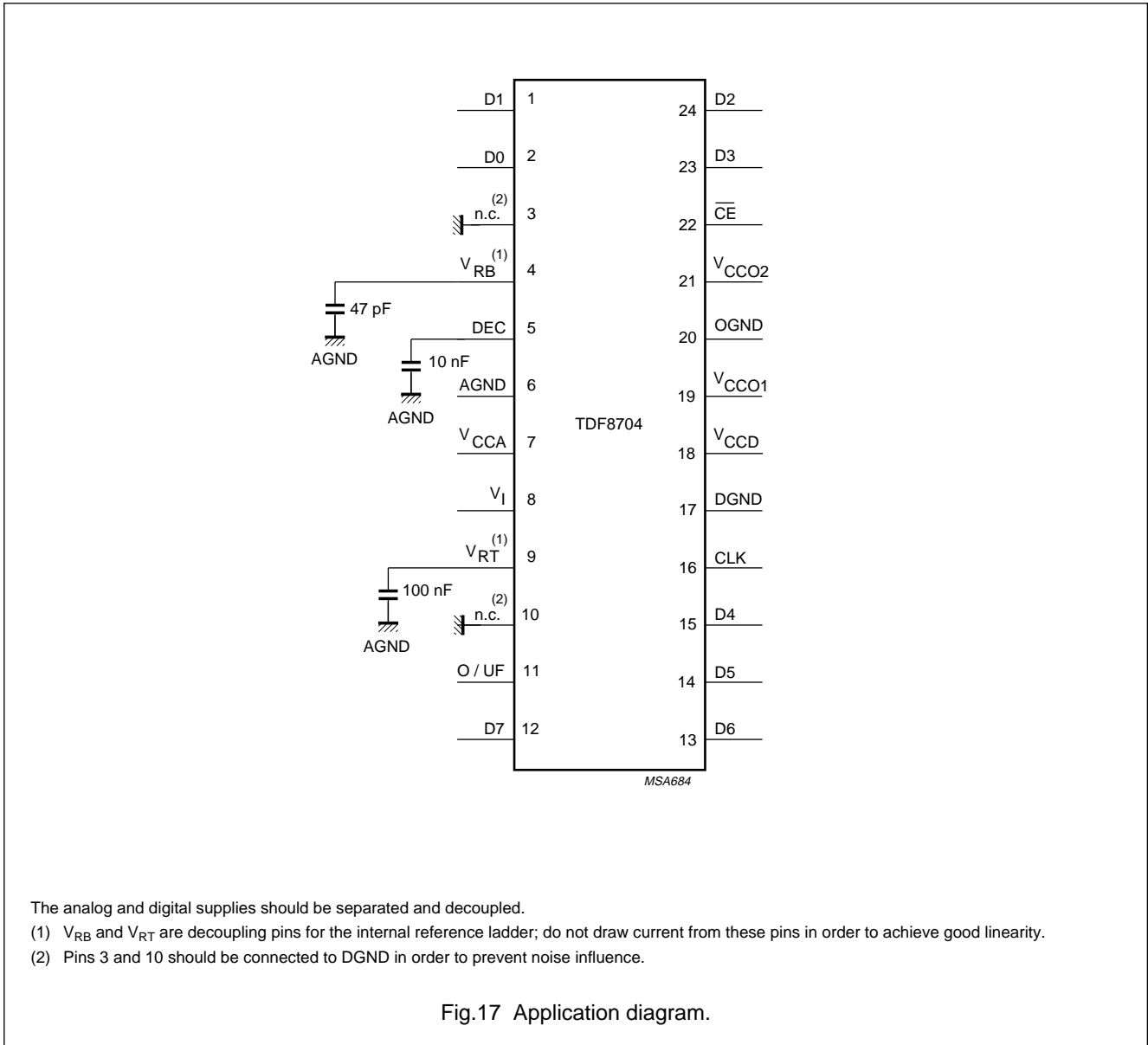


Fig.16 CLK input.

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APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.  
 (1) V<sub>RB</sub> and V<sub>RT</sub> are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.  
 (2) Pins 3 and 10 should be connected to DGND in order to prevent noise influence.

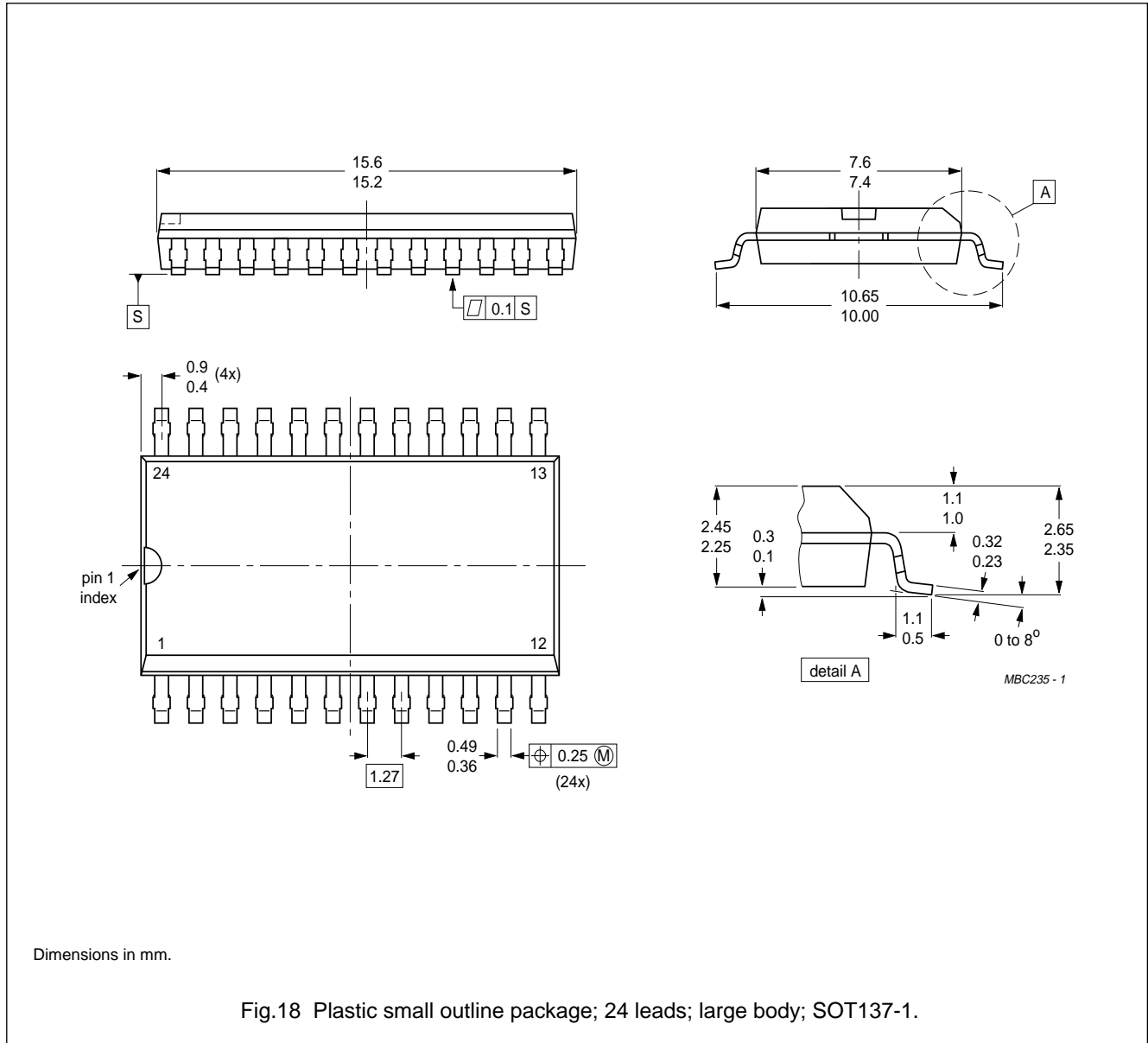
Fig.17 Application diagram.



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PACKAGE OUTLINE



## 8-bit high-speed analog-to-digital converter

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**SOLDERING****Plastic small-outline packages**

## BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

## BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be

applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

**REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)**

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

8-bit high-speed analog-to-digital converter

TDF8704

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